Problem 1)

```
       A=32'b0101_0101_0101_0101_0101_0101_0101_0101;
       B=32'b0101_0101_0101_0101_0101_0101_0101_0101;

VCD info: dumpfile MIPSAlu.vcd opened for output.
                  0 A = 55555555 B = 55555555 ALUOut = 00000000 Zero = 1
                 10 A = 55555555 B = 55555555 ALUOut = 55555555 Zero = 0
                 30 A = 55555555 B = 55555555 ALUOut = aaaaaaaa Zero = 0
                 40 A = 55555555 B = 55555555 ALUOut = 00000000 Zero = 1


      A=32'b0000_0000_0000_0000_0000_0000_0000_0000;
      B=32'b0000_0000_0000_0000_0000_0000_0000_0000;

VCD info: dumpfile MIPSAlu.vcd opened for output.
                  0 A = 00000000 B = 00000000 ALUOut = 00000000 Zero = 1


      A=32'b0000_0000_0000_0000_0000_0000_0000_1111;
      B=32'b0000_0000_0000_0000_0000_0000_0000_0001;
VCD info: dumpfile MIPSAlu.vcd opened for output.
                  0 A = 0000000f B = 00000001 ALUOut = 00000000 Zero = 1
                 10 A = 0000000f B = 00000001 ALUOut = 00000001 Zero = 0
                 20 A = 0000000f B = 00000001 ALUOut = 0000000f Zero = 0
                 30 A = 0000000f B = 00000001 ALUOut = 00000010 Zero = 0
                 40 A = 0000000f B = 00000001 ALUOut = 0000000e Zero = 0
```

The main experiment here was changing A and B to see how the ALU works.

Problem 2)

(no nops added)

```
VCD info: dumpfile test_mipspipe.vcd opened for output.


clock cycle =  1 (time = 10)
IF/ID registers
         IF/ID.PC+4 = 00000004, IF/ID.IR = 00412820

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = xxxxxxxx, EX/MEM.ALUout = xxxxxxxx
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = xxxxxxxx
         EX/MEM.op = 00
```

```
clock cycle =  2 (time = 20)
IF/ID registers
         IF/ID.PC+4 = 00000008, IF/ID.IR = 8ca30004

ID/EX registers
         ID/EX.rs =  2, ID/EX.rt =  1
         ID/EX.A = 00000002, ID/EX.B = 00000001
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  2, EX/MEM.rt =  1
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = xxxxxxxx
         EX/MEM.op = 00



clock cycle =  3 (time = 30)
IF/ID registers
         IF/ID.PC+4 = 0000000c, IF/ID.IR = 8c420000

ID/EX registers
         ID/EX.rs =  5, ID/EX.rt =  3
         ID/EX.A = 00000005, ID/EX.B = 00000003
         ID/EX.op = 23

EX/MEM registers
         EX/MEM.rs =  5, EX/MEM.rt =  3
         EX/MEM.ALUOut = 00000003, EX/MEM.ALUout = 00000001
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle =  4 (time = 40)
IF/ID registers
         IF/ID.PC+4 = 00000010, IF/ID.IR = 00a31825

ID/EX registers
         ID/EX.rs =  2, ID/EX.rt =  2
         ID/EX.A = 00000002, ID/EX.B = 00000002
         ID/EX.op = 23

EX/MEM registers
         EX/MEM.rs =  2, EX/MEM.rt =  2
         EX/MEM.ALUOut = 00000009, EX/MEM.ALUout = 00000003
         EX/MEM.op = 23

MEM/WB registers
         MEM/WB.rd =  5, MEM/WB.rt =  1
         MEM/WB.value = 00000003
         EX/MEM.op = 00
```

```
clock cycle =  5 (time = 50)
IF/ID registers
         IF/ID.PC+4 = 00000014, IF/ID.IR = aca30000

ID/EX registers
         ID/EX.rs =  5, ID/EX.rt =  3
         ID/EX.A = 00000005, ID/EX.B = 00000003
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  5, EX/MEM.rt =  3
         EX/MEM.ALUOut = 00000002, EX/MEM.ALUout = 00000002
         EX/MEM.op = 23

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  3
         MEM/WB.value = 00000000
         EX/MEM.op = 23



clock cycle =  6 (time = 60)
IF/ID registers
         IF/ID.PC+4 = 00000018, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  5, ID/EX.rt =  3
         ID/EX.A = 00000003, ID/EX.B = 00000003
         ID/EX.op = 2b

EX/MEM registers
         EX/MEM.rs =  5, EX/MEM.rt =  3
         EX/MEM.ALUOut = 00000007, EX/MEM.ALUout = 00000003
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  2
         MEM/WB.value = 00000000
         EX/MEM.op = 23



clock cycle =  7 (time = 70)
IF/ID registers
         IF/ID.PC+4 = 0000001c, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000003, EX/MEM.ALUout = 00000003
         EX/MEM.op = 2b

MEM/WB registers
         MEM/WB.rd =  3, MEM/WB.rt =  3
         MEM/WB.value = 00000007
         EX/MEM.op = 00
```

```
clock cycle =  8 (time = 80)
IF/ID registers
         IF/ID.PC+4 = 00000020, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  3
         MEM/WB.value = 00000007
         EX/MEM.op = 2b



clock cycle =  9 (time = 90)
IF/ID registers
         IF/ID.PC+4 = 00000024, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle = 10 (time = 100)
IF/ID registers
         IF/ID.PC+4 = 00000028, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00
```

```
clock cycle = 11 (time = 110)
IF/ID registers
         IF/ID.PC+4 = 0000002c, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle = 12 (time = 120)
IF/ID registers
         IF/ID.PC+4 = 00000030, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle = 13 (time = 130)
IF/ID registers
         IF/ID.PC+4 = 00000034, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
```

```
         EX/MEM.op = 00



clock cycle = 14 (time = 140)
IF/ID registers
         IF/ID.PC+4 = 00000038, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle = 15 (time = 150)
IF/ID registers
         IF/ID.PC+4 = 0000003c, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle =  0 (time = 160)
```

(nops added)

```
VCD info: dumpfile test_mipspipe.vcd opened for output.


clock cycle =  1 (time = 10)
IF/ID registers
         IF/ID.PC+4 = 00000004, IF/ID.IR = 00412820

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00
```

```
EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = xxxxxxxx, EX/MEM.ALUout = xxxxxxxx
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = xxxxxxxx
         EX/MEM.op = 00



clock cycle =  2 (time = 20)
IF/ID registers
         IF/ID.PC+4 = 00000008, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  2, ID/EX.rt =  1
         ID/EX.A = 00000002, ID/EX.B = 00000001
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  2, EX/MEM.rt =  1
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = xxxxxxxx
         EX/MEM.op = 00



clock cycle =  3 (time = 30)
IF/ID registers
         IF/ID.PC+4 = 0000000c, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000003, EX/MEM.ALUout = 00000001
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle =  4 (time = 40)
IF/ID registers
         IF/ID.PC+4 = 00000010, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
```

```
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  5, MEM/WB.rt =  1
         MEM/WB.value = 00000003
         EX/MEM.op = 00



clock cycle =  5 (time = 50)
IF/ID registers
         IF/ID.PC+4 = 00000014, IF/ID.IR = 8ca30004

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle =  6 (time = 60)
IF/ID registers
         IF/ID.PC+4 = 00000018, IF/ID.IR = 8c420000

ID/EX registers
         ID/EX.rs =  5, ID/EX.rt =  3
         ID/EX.A = 00000003, ID/EX.B = 00000003
         ID/EX.op = 23

EX/MEM registers
         EX/MEM.rs =  5, EX/MEM.rt =  3
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle =  7 (time = 70)
IF/ID registers
         IF/ID.PC+4 = 0000001c, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  2, ID/EX.rt =  2
```

```
         ID/EX.A = 00000002, ID/EX.B = 00000002
         ID/EX.op = 23

EX/MEM registers
         EX/MEM.rs =  2, EX/MEM.rt =  2
         EX/MEM.ALUOut = 00000007, EX/MEM.ALUout = 00000003
         EX/MEM.op = 23

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle =  8 (time = 80)
IF/ID registers
         IF/ID.PC+4 = 00000020, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000002, EX/MEM.ALUout = 00000002
         EX/MEM.op = 23

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  3
         MEM/WB.value = ffffffff
         EX/MEM.op = 23



clock cycle =  9 (time = 90)
IF/ID registers
         IF/ID.PC+4 = 00000024, IF/ID.IR = 00a31825

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  2
         MEM/WB.value = 00000000
         EX/MEM.op = 23



clock cycle = 10 (time = 100)
IF/ID registers
         IF/ID.PC+4 = 00000028, IF/ID.IR = 00000020

ID/EX registers
```

```
         ID/EX.rs =  5, ID/EX.rt =  3
         ID/EX.A = 00000003, ID/EX.B = ffffffff
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  5, EX/MEM.rt =  3
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle = 11 (time = 110)
IF/ID registers
         IF/ID.PC+4 = 0000002c, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = ffffffff, EX/MEM.ALUout = ffffffff
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle = 12 (time = 120)
IF/ID registers
         IF/ID.PC+4 = 00000030, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  3, MEM/WB.rt =  3
         MEM/WB.value = ffffffff
         EX/MEM.op = 00



clock cycle = 13 (time = 130)
IF/ID registers
         IF/ID.PC+4 = 00000034, IF/ID.IR = aca30000
```

```
ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle = 14 (time = 140)
IF/ID registers
         IF/ID.PC+4 = 00000038, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  5, ID/EX.rt =  3
         ID/EX.A = 00000003, ID/EX.B = ffffffff
         ID/EX.op = 2b

EX/MEM registers
         EX/MEM.rs =  5, EX/MEM.rt =  3
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle = 15 (time = 150)
IF/ID registers
         IF/ID.PC+4 = 0000003c, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000003, EX/MEM.ALUout = ffffffff
         EX/MEM.op = 2b

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00



clock cycle =  0 (time = 160)
```

nops were added after many of the operations because many of the operations take multiple cycles and some instructions access the same data, creating data hazards.

The experiment involved adding basic MIPS instructions to a Verilog system to see how systems work both with data hazards and with mitigated hazards.